REMARKS

Introduction

This amendment is submitted in response to the Office Action dated January 2, 2004, in the present application. Claims 1-16 and 44-47 were previously in the application (claims 17-40 having been previously withdrawn). In the Office Action, claims 1-16 and 44-47 were rejected. By the present Amendment, applicants have amended claims 1, 7 and 13, and cancelled without prejudice previously withdrawn claims 17-40. Accordingly, claims 1-16 and 44-47 are presently in the application. Claims 1, 7 and 13 are independent.

Objection to the Specification

In the Office Action, the Abstract was objected to for containing more than 150 words. By this Amendment, applicants have amended the abstract to contain less than 150 words. Accordingly, withdrawal of the objection is respectfully requested.

Rejections Under 35 U.S.C. §102

In the Office Action, claims 1-4, 6-8, 10, 11, 13, 15, 16 and 41-43 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,767,792 to Urbas, et al. ("Urbas").

Urbas (which shares inventors with, and has the same assignee as the present application) discloses a transponder and interrogator system wherein the transponder includes an antenna for receiving an input signal to power the transponder, the signal also containing data and commands from the signal source and being also capable of transmitting an output signal to

the interrogator. The transponder also includes memory for storing data received by the transponder. Urbas describes that as the OUTPUT ENABLE goes low, it tri-states the **output** of EEPROM 25 so as not to conflict with data from buffer 9 and/or multiplexor 9A on data bus 30. See Urbas at FIG. 1 and col. 7, lns. 57-60.

Claim 1, as amended, of the present application is directed to a transponder comprising a memory for storing data therein, a clock generator for outputting a read signal for supplying current to the memory, and an address module for addressing a selected address from a plurality of addresses in the memory. The clock generator outputs an increase address signal and the address module selects an address to be read in response to the increase address signal from the clock generator. The transponder also comprises a data module receiving the data stored in the memory at the selected address indicated by the address module and for latching the data in response to a latch data signal from the clock generator, the clock generator stopping supplying the read signal to turn off the current to the memory each time the contents of a selected memory address from the plurality of addresses are output from the memory to the data module, the current thus being cycled on and off with each latching of the contents of each successive selected memory address in the data module.

Applicants respectfully submit that Urbas does not describe all of the features as recited by claim 1, as amended, of the present application. For example, while claim 1 recites the clock generator stopping supplying the read signal to turn off the current to the memory each time the contents of a selected memory address from the plurality of addresses are output from the memory to the data module, the current thus being cycled on and off with each latching of the contents of each successive selected memory address in the data module, Urbas does not describe

any such cycling of the current on and off with each latching of the contents of each successive selected memory address in the data module. While Urbas does describe the output of an EEPROM having a tri-state configuration, such a tri-state output is very different than the features recited by claim 1 of the present application, wherein a clock generator stops supplying the read signal to turn off the current to the memory each time the contents of a selected memory address from the plurality of addresses are output from the memory to the data module.

A benefit of the claimed invention of claim 1 of the present application is that the claimed transponder, by stopping supplying the read signal to turn off the current to the memory each time the contents of a selected memory address from the plurality of addresses are output from the memory to the data module, can achieve a stated object of embodiments of the claimed invention, which is "to provide a transponder which minimizes power used during programming and reading of the transponder." Present Specification at Page 3, lines 22-23.

As further described in the Specification of the present Application:

> During the READ MODE, clock generator 36 provides a READ EEPROM signal to memory 28. As READ EEPROM signal is input to memory 28, memory 28 is utilizing current. **However, during operation of a preferred embodiment, the READ EEPROM signal is output to memory 28 only while address module 38 latches the address in memory 28 and data is output to data module 40. Once the data is output along the DATA BUS, the READ EEPROM signal is disabled until clock generator 36 outputs a successive INCR ADDR signal to increase the address to be addressed by the address module 38. The READ EEPROM signal is then enabled and current is supplied to memory 28 to allow reading of data in memory 28 and this process is repeated until the READ MODE is terminated when power is removed from transponder 20. By cutting off the current supply to memory 28, the overall current consumed during the READ MODE is lowered.** Because the memory is in EEPROM, i.e., a static memory, the data

> is stored even in the absence of current being supplied to memory 28.

Present Specification at Page 12, lines 4-16. (Emphasis Added).

Thus, by inventively turning off the current to the memory each time the contents of a selected memory address from the plurality of addresses are output from the memory to the data module, a benefit of the claimed invention can be realized, namely the lowering of overall current consumed. In contrast, in the system described by Urbas, as would be known to one of ordinary skill in the art, the intention of tri-stating the output (not the claimed turning off an input) of the memory is to allow other devices to output data to a data bus, and not the saving of power. For example, an informal Internet search performed at Google.com using the search term tri-state resulted in a document entitled "What's a Tri-State Buffer" (http://www.cs.umd.edu/class/spring2003/cmsc311/Notes/CompOrg/tristate.html, a copy of which is annexed hereto). That document states:

> a common way for many devices to communicate with one another is on a bus, and that a bus should only have one device writing to it, although it can have many devices reading from it.
>
> Since many devices always produce output (such as registers) and these devices are hooked to a bus, we need a way to control what gets on the bus, and what doesn't.

Id. at page 4 of 5, ¶¶ 6-7.

Thus, Urbas does not describe the claimed transponder wherein a clock generator stops supplying the read signal to turn off the current to the memory each time the contents of a selected memory address from the plurality of addresses are output from the memory to the data module. In addition, Urbas does not describe a transponder whereby the beneficial results of

minimizing power used during programming and reading of the transponder in the same manner as that of the claimed invention.

Further, claim 1 of the present invention recites the clock generator stopping supplying the read signal to turn off the current to the memory. In stark contrast, Urbas discloses tri-stating the data output of EEPROM 25 so as not to conflict with data from buffer 9 and/or multiplexor 9A on data bus 30. Generally, as is known by those skilled in the art, when an output is "tri stated," it is set to a high-impedance condition. This allows other outputs to drive signals onto the shared data bus 30 without conflicting data outputs. The tri-stating of the output of the EEPROM of Urbas is very different from the stopping of current to the memory as recited by claim 1 of the present application. In fact, tri-stating an output does not imply turning off current to a circuit; the maintaining of a high impedance output state may require current to a circuit. Thus, for this additional reason, applicants submit that Urbas does not describe the claimed invention.

Accordingly, applicants respectfully submit that Urbas does not disclose all of the features as recited by claim 1 of the present application. Accordingly, applicants request that the Examiner withdraw the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-4, 6, 11, 16, 44 and 45 depend, either directly or indirectly, from claim 1. Accordingly, applicants respectfully submit that, for the reasons stated above with respect to the rejection of claim 1, claims 2-4, 6, 11, 44 and 45 are allowable, at least for depending from allowable claim 1. Accordingly, applicants respectfully request that the examiner withdraw the rejections to claims 2-4, 6, 11, 16, 44 and 45 based on 35 U.S.C. §102(b).

Claim 7, as amended, of the present application claims a transponder similar to that claimed by claim 1, discussed above, of the present application. Specifically, claim 7 recites, *inter alia*, a transponder comprising: a memory for storing data therein, the memory having addresses, a clock generator outputting a program signal for supplying current to the memory to program the memory, and an address module for addressing a selected address from a plurality of addresses in the memory. The clock generator outputs an address latched signal, the address module selecting a selected address to be read in response to the address latch signal. The transponder also comprises a data module for inputting data to the memory at the address indicated by the address module, the clock generator stopping supplying current to the memory each time the contents of a selected memory address from the plurality of addresses has been stored in the memory, the current thus being cycled on and off with each storing of the contents of each successive selected memory address of the plurality of memory addresses in the memory.

As stated above with respect to the rejections to claim 1 of the present application, Urbas does not describe a clock generator stopping supplying current to the memory each time the contents of a selected memory address from the plurality of addresses has been stored in the memory, the current thus being cycled on and off with each storing of the contents of each successive selected memory address of the plurality of memory addresses in the memory.

Accordingly, applicants respectfully submit that Urbas does not disclose all of the features as recited by claim 7 of the present application, and applicants request that the Examiner withdraw the rejection to claim 7 under 35 U.S.C. §102(b).

Claims 8 and 10 depend, either directly or indirectly, from claim 7. Accordingly, applicants respectfully submit that, for the reasons stated above with respect to the rejection of

claims 1 and 7, claims 8 and 10 are allowable, at least for depending from allowable claim 7. Accordingly, applicants respectfully request that the examiner withdraw the rejections to claims 8 and 10 based on 35 U.S.C. §102(b).

Claim 13 has, as amended, recites, *inter alia*, a transponder comprising a memory, the memory including a data region and a status byte region, a clock generator for receiving a program signal and outputting a data latch signal in response thereto, an address module for receiving the address latch signal and addressing a predetermined address from a plurality of addresses in the memory to be programmed, and a program control for reading the status byte and outputting a program enable signal in response thereto. The clock generator receives the program enable signal and outputs the address latch in response to the program enable signal. A data module receives the data stored in the memory at an address indicated by the address module, the clock generator stopping supplying the read signal to turn off the current to the memory each time the data from a predetermined address has been output to the data module, the current thus being cycled on and off with each outputting of the data of each successive address of the plurality of addresses.

As stated above with respect to similar features of claims 1 and 7 in the discussion of the rejections to claims 1 and 7, applicants respectfully submit that Urbas does not disclose a the clock generator stopping supplying the read signal to turn off the current to the memory each time the data from a predetermined address has been output to the data module, the current thus being cycled on and off with each outputting of the data of each successive address of the plurality of addresses.

Accordingly, applicants respectfully submit that Urbas does not disclose all of the features as recited by claim 13, as amended, of the present application, and applicants request that the Examiner withdraw the rejection to claim 13 under 35 U.S.C. §102(b).

Claim 15 depends from claim 13. Accordingly, applicants respectfully submit that, for the reasons stated above with respect to the rejection of claims 1 and 7 and 13, claim 15 is allowable, at least for depending from allowable claim 13. Accordingly, applicants respectfully request that the examiner withdraw the rejection to claim 15 based on 35 U.S.C. §102(b).

Rejections Under 35 U.S.C. §103

In the Office Action, claims 5, 9, 12 and 14 were rejected under 35 U.S.C. §103(a) based on a hypothetical proposed combination of Urbas, and U.S. Patent No. 5,767,792 to Carroll et al. ("Carroll")

Applicants respectfully traverse that rejection. In the first instance, there is no teaching or suggestion in the references to make the hypothetical combination proposed in the Office Action, and thus the combination is improper.

Dependent claims 5 and 12 depend either directly or indirectly from claim 1 while, dependent claim 9 depends from claim 7, and dependent claim 14 depends from claim 13. Claims 8 and 10 depend, either directly or indirectly, from claim 7. Accordingly, applicants respectfully submit that, for the reasons stated above with respect to the rejection of claims 1 and 7, claims 8 and 10 are allowable, at least for depending from allowable claim 7. Accordingly,

applicants respectfully request that the examiner withdraw the rejections to claims 8 and 10 based on 35 U.S.C. §102(b).

Furthermore, Carroll fails to cure that deficiency. Carroll discloses a passive FR transponder and interrogator, wherein the interrogator and the transponder communicate via phase shift keying (PSK) modulation. Carroll does not describe, as part of a transponder, the advantageous feature of a clock generator stopping supplying current to the memory once the data in the data module has been stored in the memory.

Thus, applicants respectfully submit that the invention recited by claims 5, 9, 12 and 14 is not rendered obvious by the proposed hypothetical combination of Urbas and Carroll. Applicants thus respectfully submit that the invention recited by claims 5, 9, 12 and 14 is patentable over the proposed hypothetical combination of Urbas and Carroll and respectfully requests that the rejection of those claims under 35 U.S.C. §103(a) be withdrawn.

In the Office Action, claims 44-47 were rejected under 35 U.S.C. §103(a) based on a hypothetical proposed combination of Urbas, Carroll and U.S. Patent No. 5,978,192 to Young et al. ("Young").

Applicants respectfully traverse that rejection. In the first instance, there is no teaching or suggestion in the references to make the hypothetical combination proposed in the Office Action, and thus the combination is improper.

By the present Amendment, claim 46 has been amended to depend from claim 1. accordingly, claims 44-47 depend, either directly or indirectly, from claim 1. Accordingly, applicants respectfully submit that, for the reasons stated above with respect to the rejection of claim 1, claims 44-47 are allowable over Urbas, at least for depending from allowable claim 1.

Furthermore, Carroll fails to cure that deficiency. As discussed above, Carroll discloses a passive FR transponder and interrogator, wherein the interrogator and the transponder communicate via phase shift keying (PSK) modulation. Carroll does not describe, as part of a transponder, the advantageous feature of a clock generator stopping supplying current to the memory once the data in the data module has been stored in the memory.

Moreover, Young further fails to cure the deficiency. Young discloses Schmitt trigger-configured ESD protection circuit to facilitate the protection of electronic circuits from electrical surges. Young does not describe, as part of a transponder, the advantageous feature of a clock generator stopping supplying current to the memory once the data in the data module has been stored in the memory.

Thus, applicants respectfully submit that the invention recited by claims 44-47 is not rendered obvious by the proposed hypothetical combination of Urbas, Carroll and Young. Applicants thus respectfully submit that the invention recited by claims 44-47 is patentable over the proposed hypothetical combination of Urbas, Carroll and Young and respectfully request that those rejections be withdrawn.

Conclusion

Accordingly, applicants submit that all of the claims in the application (i.e., 1-16 and 44-47) are in condition for allowance.

Any fees or charges required at this time and in connection with the present application may be charged to Deposit Account No. 19-4709.

Applicants respectfully request entry of this Amendment, and early and favorable action in the above-identified application.

Respectfully submitted,

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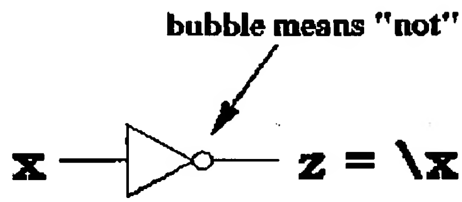
What's a Tri-state Buffer?

Introduction

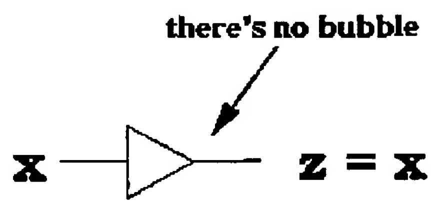
Before we talk about tri-state buffers, let's talk about an *inverter*. You can read about inverters in the notes about Logic Gates. However, we'll repeat it here for completeness.

An *inverter* is called a NOT gate, and it looks like:



The inverter is a triangle, followed by a circle/bubble. That circle sometimes appears by itself, and means negation.

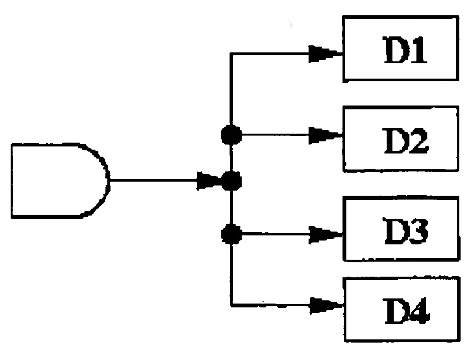
What if we remove the circle? What kind of gate would we have? We'd have a *buffer*.



You might think that a buffer is useless. After all, the output is exactly the same as the input. What's the point of such a gate?

The answer is a practical issue from real circuits. As you may know, logic gates process 0's and 1's. 0's and 1's are really electric current at certain voltages. If there isn't enough current, it's hard to measure the voltage.

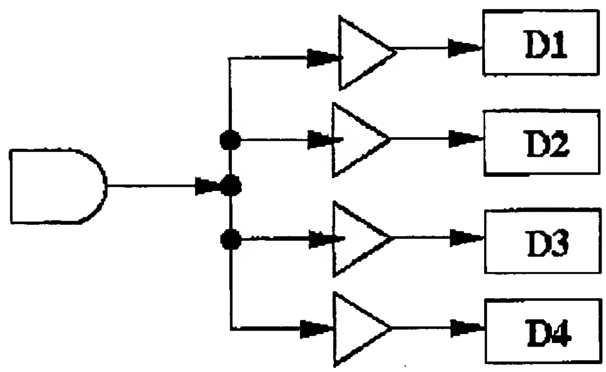
The current can decrease if the fan out is large. Here's an example:



The "fan out" is the number of devices that an output is attached to. Thus, the AND gate above is attached to the inputs of four other devices. It has a fan out of 4.

If the current coming out of the AND gate is **i**, then assuming each of the four devices gets equal current, then each device gets **i / 4** of the current.

However, if we put in a buffer:



then the current can be "boosted" back to the original strength. Thus, a buffer (like all logic gates) is an *active* device. It requires additional inputs to power the gate, and provide it voltage and current.

You might wonder "Do I really need to know this? Isn't this just EE stuff?". That's true, it is. The point of the discussion was to motivate the existence of a plain buffer.

Tri-state buffer: It's a Valve

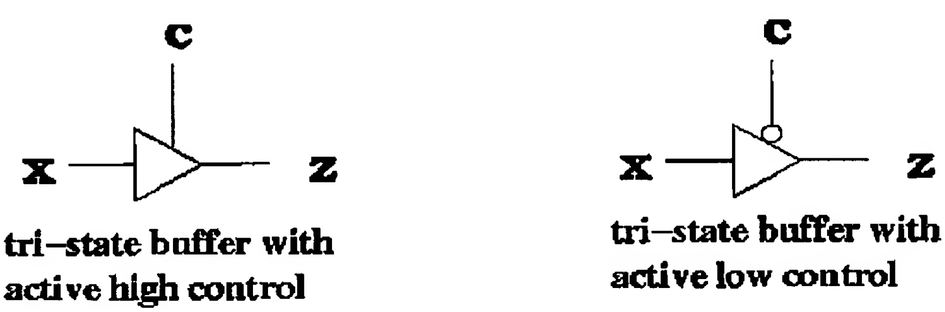
A buffer's output is defined as **z** = **x**. Thus, if the input, **x** is 0, the output, **z** is 0. If the input, **x** is 1, the output, **z** is 1.

It's a common misconception to think that 0 is nothing, while 1 is something. In both cases, they're something. If you read the discussion in What's a Wire, you'll see that a wire either transmits a 0, a 1, or "Z", which is really what's nothing.

It's useful to think of a wire as a pipe, and 0 as "red kool aid" and 1 as "green kool aid" and "Z" as "no kool aid".

A *tri-state* buffer is a useful device that allows us to control when current passes through the device, and when it doesn't.

Here's two diagrams of the tri-state buffer.



A tri-state buffer has two inputs: a data input **x** and a control input **c**. The control input acts like a valve. When the control input is active, the output is the input. That is, it behaves just like a normal buffer. The "valve" is open.

When the control input is not active, the output is "Z". The "valve" is open, and no electrical current flows through. Thus, even if **x** is 0 or 1, that value does not flow through.

Here's a truth table describing the behavior of a active-high tri-state buffer.

c	x	z
0	0	Z
0	1	Z
1	0	0
1	1	1

In this case, when the output is Z, that means it's high impedance, neither 0, nor 1, i.e., no current.

As usual,the condensed truth table is more enlightening.

c	z
0	Z
1	x

As you can see, when **c** = **1** the valve is open, and **z** = **x**. When **c** = **0** the valve is closed, and **z** = **Z** (e.g., high impedance/no current).

Active-low tri-state buffers

Some tri-state buffers are active low. In an active-low tri-state buffer, **c** = **0** turns open the valve, while **c** = **1** turns it off.

Here's the condensed truth table for an active-low tri-state buffer.

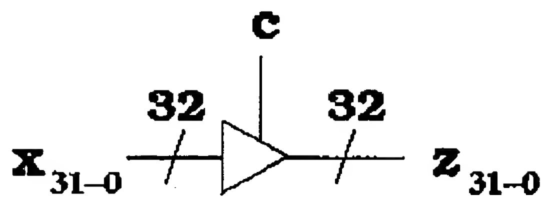
c	z
0	x
1	Z

As you can see, when **c** = **0** the valve is open, and **z** = **x**. When **c** = 1 the valve is closed, and **z** = **Z** (e.g., high impedance/no current). Thus, it has the opposite behavior of a tri-state buffer.

Multi-bit Tri-State Buffers

So far, we've talked about a tri-state buffer controlling the output of a single wire. However, it's more common to deal with many wires.

Here's an example:



tri-state buffer with
a bus of 32 bits

In this case, we have 32 wires coming into the tri-state buffer. We have 32 wires coming out of the tri-state buffer.

There's still only 1 control bit.

This can easily be implemented using 32 tri-state buffers taking one bit as input and one bit as output.

Why Tri-State Buffers?

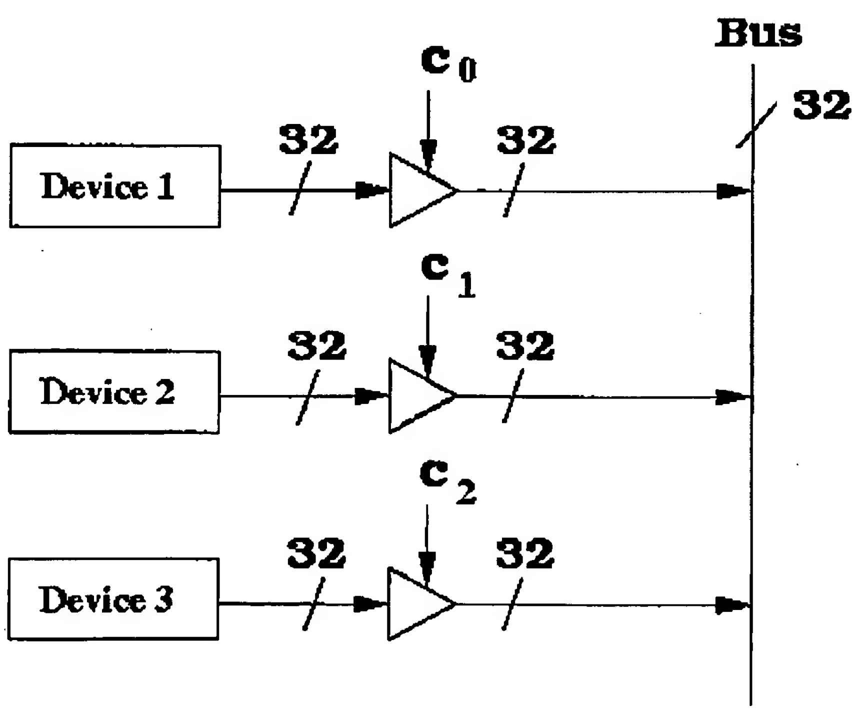
We've had a long discussion about *what* a tri-state buffer is, but not about what such a device is good for.

Recall (from earlier) that a common way for many devices to communicate with one another is on a bus, and that a bus should only have one device writing to it, although it can have many devices reading from it.

Since many devices always produce output (such as registers) and these devices are hooked to a bus, we need a way to control what gets on the bus, and what doesn't.

A tri state buffer is good for that.

Here's an example:



There are three devices, each of which output 32 bits. These devices have their outputs hooked to a 32 bit bus.

We want to prevent more than one device from writing to the bus. Ordinarily, these devices always generate output, so we're in trouble merely by attaching more than one device's output to the bus.

As long as at most one of the following control bits, c_0, c_1, c_2, is 1, the bus is fine. That is, the bus will not have two devices attempting to write to it at the same time.

Alternative: Using a MUX

Tri-state buffers are one way of preventing an output from making it to the bus.

An alternate way is to use a MUX. For example, we might have a 32 bit, 3-1 MUX. The advantage of a MUX is that we're guaranteed only one device makes it to the bus. The drawback is that we might want no devices to make it to the bus.

One solution is to add an **enable** input to a MUX. When the enable is active, the output is selected from one of the inputs. When the enable is not active, then the output is Z.

Summary

A tri-state buffer is a device that allows you to control when an output signal makes it to the bus. When the tri-state buffer's control bit is active, the input of the device makes it to the output. This is when the "valve" is open.

When it's not active, the output of the device is Z, which is high-impedance or, equivalently, nothing. This is when the "valve" is closed, and no electrical signal is allowed to pass to the output.

The "valve" analogy helps make it easy to understand the behavior of a tri-state buffer.